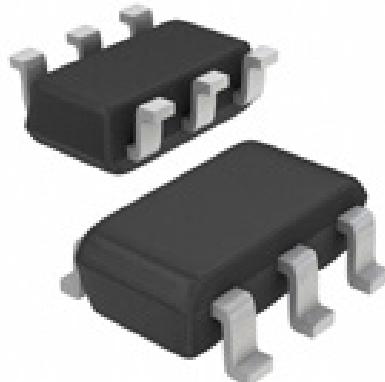


Features

- 1800Watts peak pulse power ($t_p = 8/20\mu s$)
- SOT23-6 package
- Solid-state silicon-avalanche technology
- Low clamping voltage
- Low leakage current
- Low capacitance ($C_j=1.2\text{pF}$ typ.)
- Protection one data/power line to:
- IEC 61000-4-2 $\pm 30\text{kV}$ contact $\pm 30\text{kV}$ air
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 55A (8/20 μs)



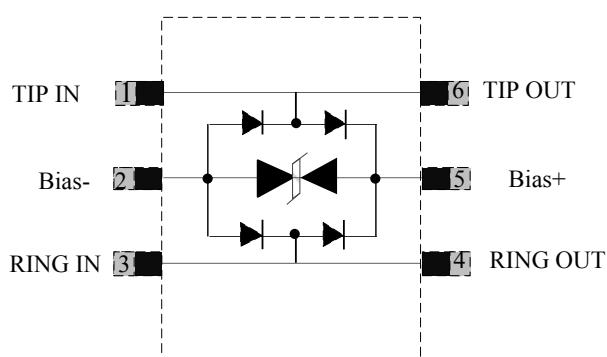
Applications

- ADSL, ADSL2+
- VDSL2, VDSL2+
- G.fast

Mechanical Data

- SOT23-6 package
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

Schematic & PIN Configuration



Absolute Maximum Rating

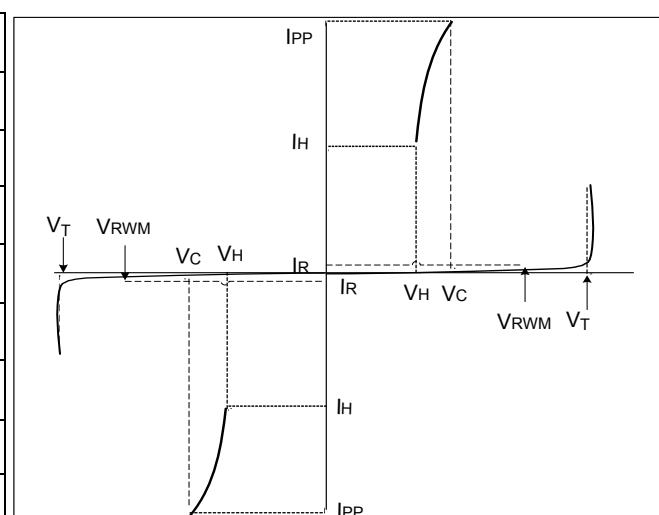
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	1800	Watts
Peak Pulse Current ($t_p = 8/20\mu s$) (note1)	I_{pp}	55	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	30 30	kV
Lead Soldering Temperature	T_L	260(10seconds)	°C
Junction Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{stg}	-55 to + 125	°C

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				8.0	V
Holding Voltage	V_H	$I_T = I_H$		3.0		V
Holding Current	I_H		50			mA
Reverse Leakage Current	I_R	$V_{RWM} = 8V, T = 25^\circ C$			500	nA
Clamping Voltage	V_C	$I_{PP} = 55A, t_p = 8/20\mu s$		35		V
Trigger Voltage	V_T			13	15	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ Line to Line		1.2		pF

Electrical Parameters (TA = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current



Note: 8/20μs pulse waveform.



Typical Characteristic Curves

Fig.1 Peak Pulse Power Rating Curve

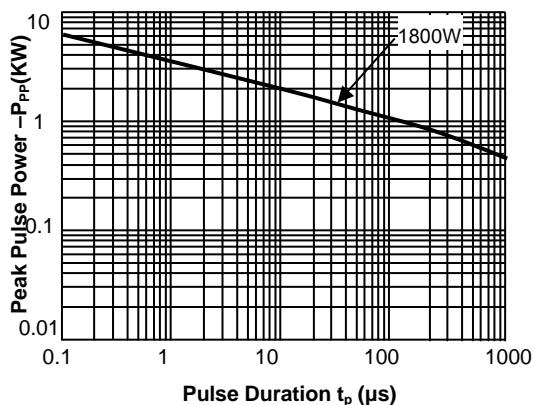


Fig.2 Pulse Derating Curve

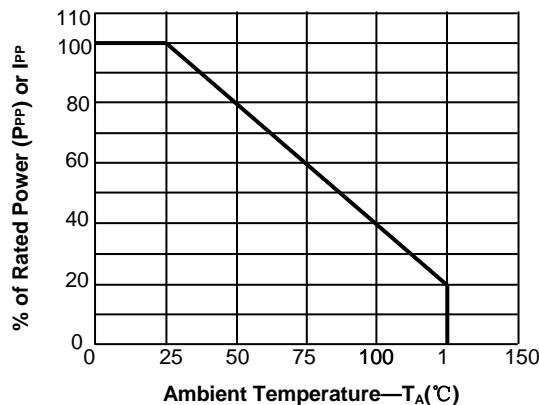


Fig.3 Pulse Waveform-8/20 μs

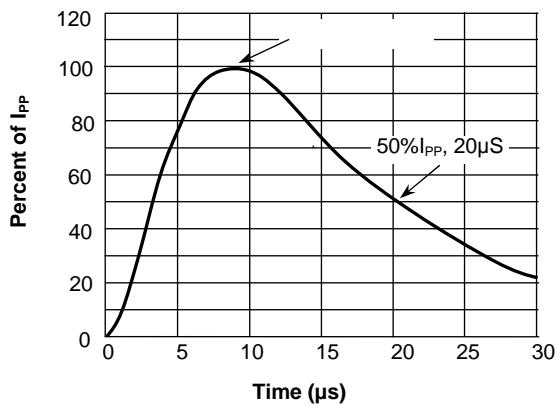
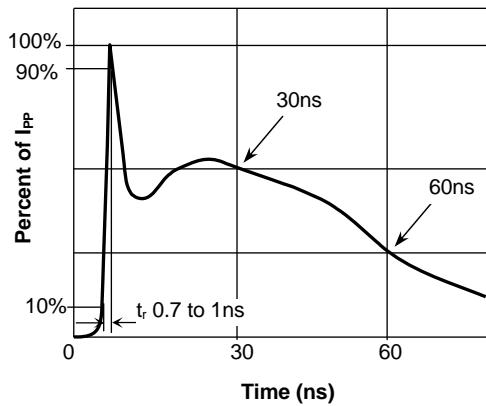


Fig.4 Pulse Waveform-ESD(IEC61000-4-2)



Application

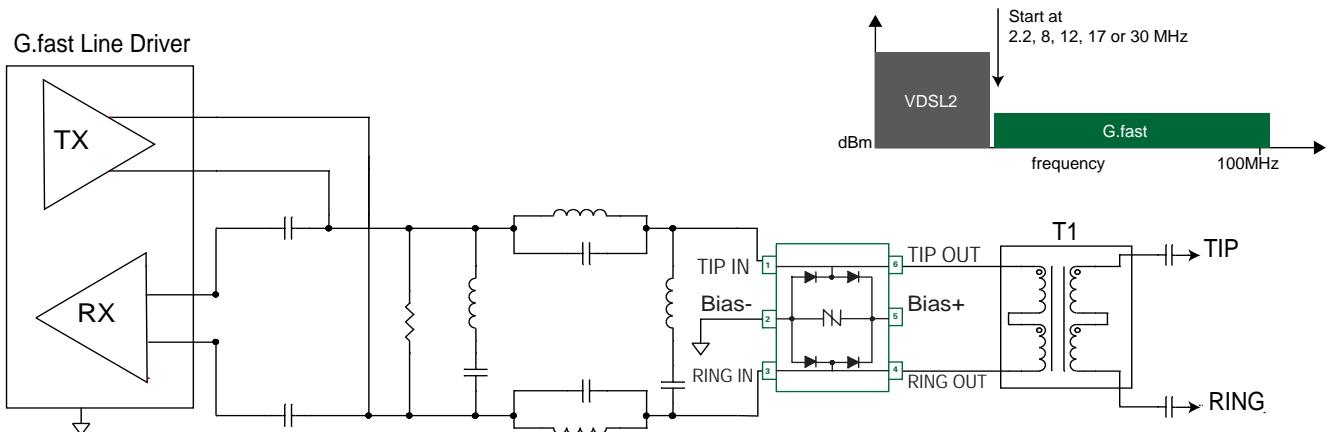


Fig.5 G.fast protection

The “Bias -” lead can be connected to the line driver ground with the “Bias +” lead left open so this solution provides both differential and common mode protection. Both “Bias -” and “Bias +” leads can be left floating for differential only protection and finally for capacitance variance sensitive applications, the “Bias -” and “Bias +” leads may have the appropriate polarity voltage (< VDRM) applied to further minimize any negative capacitance effects.



Outline Drawing – SOT23-6

PACKAGE OUTLINE		DIMENSIONS			
SYMBOL	INCHES		MILLIMETER		
	MIN	MAX	MIN	MAX	
A	0.041	0.049	1.050	1.250	
A1	0.000	0.004	0.000	0.100	
A2	0.041	0.045	1.050	1.150	
D	0.111	0.119	2.820	3.020	
E	0.059	0.067	1.500	1.700	
E1	0.104	0.116	2.650	2.950	
b	0.012	0.020	0.300	0.500	
e	0.037(BSC)		0.950(BSC)		
e1	0.071	0.079	1.800	2.000	
L	0.012	0.024	0.300	0.600	
θ	0°	8°	0°	8°	

The diagram shows a detailed land pattern for a SOT23-6 package. It includes four pads labeled with a plus sign (+). Dimensions shown are: top pad height 0.56 / 0.022, side pad height 0.95 / 0.037, side pad width 2.6 / 0.102, bottom pad height 1.0 / 0.039, bottom pad width 1.6 / 0.063, and total width 3.6 / 0.141.

Notes

- This land pattern is for reference purposes only consult your manufacturing group to ensure your company's manufacturing guidelines are met.
Reference ipc-sm-782a..

Marking**Ordering information**

Order code	Package	Base qty	Delivery mode
RLST236A082LCH	SOT23-6	3k	Tape and reel

361° Circuit Protection System

Specifications are subject to change without notice.
Please refer to <http://www.rulon.com.cn> for current information.

Revised: 2022-01-24



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